

Application Serial No: 10/761,743
Responsive to the Office Action mailed on: May 17, 2007

REMARKS

This Amendment is in response to the Office Action mailed on May 17, 2007. Claims 1, 3, 4 and 5 are cancelled without prejudice or disclaimer. Claim 7 is added and includes features of claim 1 and is further supported in the specification, for example, in Figures 1 and 4. No new matter is added. Claim 7 is pending.

§103(a) Rejections:

Claims 1-3 are rejected as being unpatentable over Morikawa (US Patent No. 5,091,818) in view of Yoshimizu (US Patent No. 5,451,814). This rejection is traversed. Claims 1-3 are cancelled without prejudice or disclaimer. Thus, this rejection is now moot. Applicants do not concede the correctness of this rejection.

Claim 4 is rejected as being unpatentable over Morikawa in view of Yoshimizu and further in view of Kawamoto (US Patent No. 6,762,461). This rejection is traversed. Claim 4 is cancelled without prejudice or disclaimer. Thus, this rejection is now moot. Applicants do not concede the correctness of this rejection.

Claim 5 is rejected as being unpatentable over Morikawa in view of Yoshimizu and further in view of Chen (US Patent Application No. 10/272,061). This rejection is traversed. Claim 5 is cancelled without prejudice or disclaimer. Thus, this rejection is now moot. Applicants do not concede the correctness of this rejection.

New Claim 7:

In order to expedite the prosecution of this matter the following is noted with respect to claim 7. Claim 7 is directed to an electronic apparatus that requires, among other features, a first IC including a first voltage input terminal, a first constant voltage input terminal, and a control block to which the voltage limited by a voltage control terminal is supplied, where a detection voltage, which is based on a constant voltage applied to the first constant voltage input terminal, is compared with a reference voltage so as to apply a control signal to the voltage control terminal based on a result of said comparison. Claim 7 also requires a control transistor, being electrically connected between the external power terminal and the first constant voltage input terminal, which is controlled by the control signal, and a second IC including a second voltage input

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terminal to which the input voltage applied to the first voltage input terminal is applied, a second constant voltage input terminal to which the constant voltage is applied, a second circuit block, being electrically connected to the second voltage input terminal, where the input voltage is supplied, and a predetermined circuit block, being electrically connected to the second constant voltage input terminal, where the constant voltage applied thereto is supplied. Claim 7 further requires that a resistor and said voltage limiting means limit an input voltage to be applied to the first voltage input terminal and the second voltage input terminal such as to have the predetermined value when the DC power voltage to be applied to the external power terminal becomes an overvoltage, and the constant voltage is supplied to a predetermined circuit block which is provided in the second IC.

The prior art references Morikawa, Yoshimizu, Kawamoto or Chen either alone or in combination do not teach or suggest these features. Morikawa is directed to an overvoltage protecting circuit but does not teach or suggest a first constant voltage input terminal, and a control block to which the voltage limited by a voltage control terminal is supplied, where a detection voltage, which is based on a constant voltage applied to the first constant voltage input terminal, is compared with a reference voltage so as to apply a control signal to the voltage control terminal based on a result of said comparison. Moreover, Morikawa also does not teach or suggest a second constant voltage input terminal to which the constant voltage is applied, a second circuit block, being electrically connected to the second voltage input terminal, where the input voltage is supplied, and a predetermined circuit block, being electrically connected to the second constant voltage input terminal, where the constant voltage applied thereto is supplied. Lastly, Morikawa also does not teach or suggest a resistor and said voltage limiting means limit an input voltage to be applied to the first voltage input terminal and the second voltage input terminal such as to have the predetermined value when the DC power voltage to be applied to the external power terminal becomes an overvoltage, and the constant voltage is supplied to a predetermined circuit block which is provided in the second IC.

Yoshimizu does not overcome these deficiencies. Yoshimizu is directed to a multi-chip module integrated circuit that has two IC chips (21, 22) connected directly to

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an input voltage (VCC). However, nowhere does Yoshimizu teach or suggest the features of claim 7 listed above.

Kawamoto also does not overcome these deficiencies. Kawamoto is directed to a semiconductor element protected with a plurality of zener diodes. However, nowhere does Yoshimizu teach or suggest the features of claim 7 listed above.

Chen also does not overcome these deficiencies. Chen is directed to a high ESD stress sustaining ESD protection circuit. However, nowhere does Chen teach or suggest the features of claim 7 listed above. For at least these reasons claim 7 is not suggested by the Morikawa, Yoshimizu, Kawamoto or Chen either alone or in combination.

Conclusion:

Applicants respectfully assert claim 7 is now in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.



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Respectfully submitted,

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